EG&G RETICON R5106 SAMPLED ANALOG DELAY LINE (Pin-compatible replacement for SAD512D)

Key Features

- 512-element delay
- On-chip driver requiring only single TTL-level clock input
- Clock-controlled delay: more than 1 sec to less than 300 μsec
- Improved N-channel silicon-gate bucket-brigade technology
- Sample-and-hold output circuit for maximum self-cancellation of clocking modulation
- Wide signal-frequency range: 0 to more than 300 KHz
- Wide sampling clock frequency range: 0.25 KHz to more than 500 KHz
- Wide dynamic range: S/N >70 dB
- Low distortion: less than 1%
- Single 12 volt power supply (5 to 13 volts range)
- 8 pin mini DIP

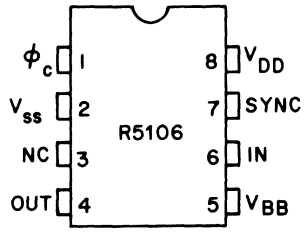

Figure 1. Pinout, R5106

R5106 Sampled Analog Delay Line

The R5106 is a general-purpose Sampled Analog Delay device fabricated using N-channel silicon gate technology in a bucket-brigade configuration. It is an improved pin-compatible replacement for the SAD-512D.

Typical Applications

- Voice control of tape recorders
- Control of equalization filters
- Reverberation effects in stereo equipment
- Tremolo, vibrato, or chorus effects in electronic musical instruments
- Variable or fixed delay of analog signals
- Time compression of telephone conversations or other analog signals
- Voice scrambling systems
- Storage of multi-level digital signals

Device Description

The R5106 is a 512-element Bucket Brigade Device (BBD) with internal clock drivers that require only a TTL-level (or higher) single-phase clock input (f_C).

A sampled-and-held output is provided for smooth stair-step output over each full clock period in normal operation. The R5106 is manufactured using an improved N-channel silicon-gate technology to fabricate a chain of MOS transistors and storage capacitors into a bucket-brigade charge-transfer device. It is packaged in a standard 8-lead dual-in-line package with pin configuration as shown in Figure 1. The functional equivalent circuit is shown in Figure 2.

Drive and Voltage Requirements

Normal voltage levels and limits are given in the tabular specifications. The clock input is a rectangular wave which controls the on-chip drivers. The magnitude of the clock may be any positive pulse voltage from 2 volts to V_{DD}. The phase relationships of clock input, sync input (when used) and output waveforms are shown in Figure 4. The input trigger clock is best as a controlled rectanguiar puise with rise and fall times less than 50 nsec. For operation at the highest frequency, it should be a square wave, but more generally, the positive portion should have a duration greater than 200 nsec (preferably greater than 500 nsec) and the low-level portion should be greater than 300 nsec. Within these broad limits, the timing is non-critical. The positive portion determines the duration of the sampling period of the output sample-and-hold so that short pulses give a cleaner output step. The low-level portion determines the input tracking interval, of minor importance so long as the duration is great enough (preferably 300-500 nsec or greater).

For optimum performance, V_{DD} is 13 volts and V_{BB} approximately 10 to 10.5 volts. However, for battery or portable operation, both may be operated at lower levels. V_{BB} is internally derived from V_{DD}, but requires an external load of approximately 20KΩ to V_{SS} (ground) to give the desired relationship between V_{DD} and V_{BB}. The input bias voltage is best derived as a (large) fraction of the V_{BB} voltage, as in the circuit sketch, Figure 3; when so derived, operating conditions track with minimum or no readjustment when V_{DD} changed, even over a wide range.

When used, the sync input should be a postive pulse of magnitude $V_{DD}/2 < V_{sync} \leq V_{DD}$, and timing as shown in Figure 4; that is, the sync input should rise 50 nsec or later after a falling edge of the trigger clock input, and fall at or before the next falling edge of the trigger clock.

If the sync input is unused, pin 7 should be connected to ground.

As with all sampled-data devices, the input bandwidth should be limited to a value less than one-half the sampling clock frequency (usually to a value less than 0.3 f_S). Further, to recover a smooth delayed analog output, a post filter having steep cutoff (e.g., 36 dB per octave or more) is desirable.

Performance

Typical performance of the device is shown in the specifications and in the curves of Figures 5 through 7. These data were obtained with the test configuration on Figure 4 or similar. Sampling waveforms, propagation delays, and internal dispersion become the limiting factors for sampling clock frequencies above 800 KHz (1.6 MHz f_C).

Figures 5 and 6 indicate the linearity and show the rapid increase in distortion as the input level is increased toward saturation. For inputs less than approximately 1.5 volts rms, the distortion is less than one percent. Between this point and the noise floor, there is approximately 75 dB of dynamic range. This dynamic range assumes an A weighting filter and a sample rate of 100 KHz or faster. With a 20 KHz filter and 50 KHz sample rate, the dynamic range is 70 dB. Broad-band dynamic range is better than 60 dB for all sample rates.

The output is internally sampled and held, then buffered by a source follower with internal load adequate to drive a capacitive load of up to 200 pF without further components. With 200 pF, the slew rate is approximately 0.5V/μsec, and is inversely proportional to the capacitance load. The slew rate is limited by the internal pull-down current of approximately 150 μA; pull up is at least an order of magnitude faster (lower in impedance). The internal current is inadequate to drive a low a-c coupled resistance without substantial increase in second harmonic. A-C coupled loads are preferably 50K or greater. Otherwise, an external buffer as in the circuit of Figure 9 is recommended.

The sampled-and-held nature of the output signal implies a frequency response of the form $[\sin(\pi f_m/f_s)]/(\pi f_m/f_s)$ independent of any transfer gain or loss of the delay line itself (f_m is the signal frequency and f_s the sample frequency). This response function is simply the amount of equivalent base-band signal in the stair-step sampled signal. Figure 7 shows its relative attenuation

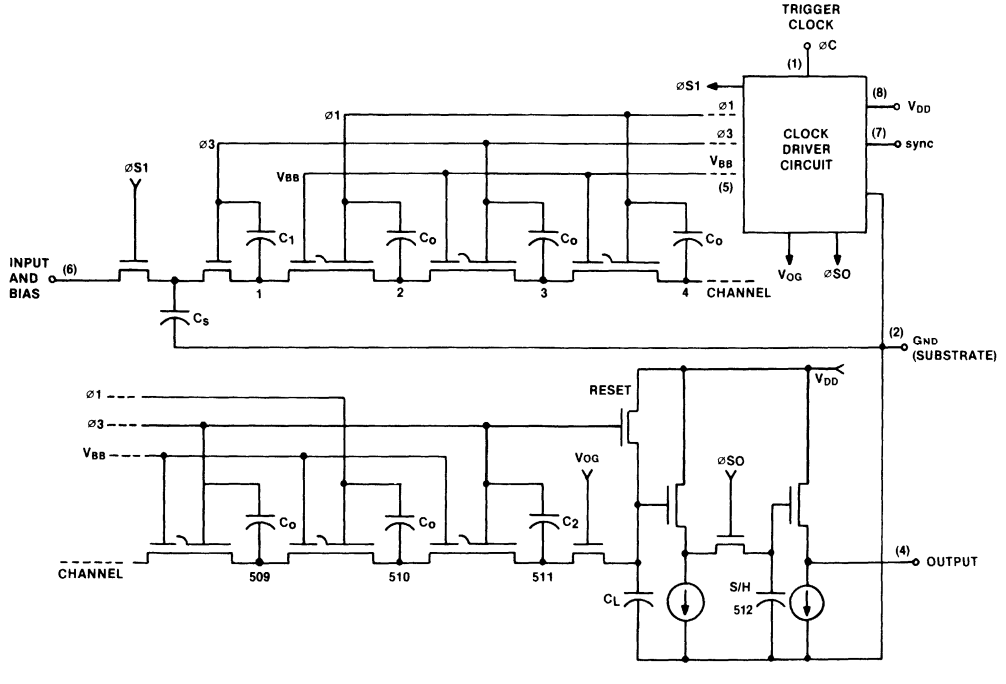

Figure 2. Equivalent Circuit of R5106

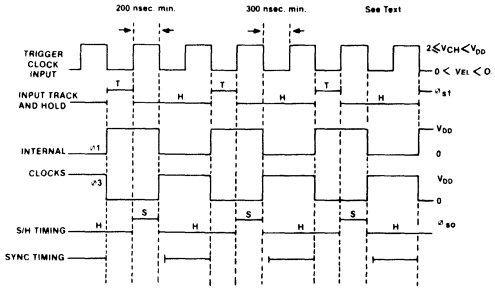

Figure 3. R5106 Timing Relations

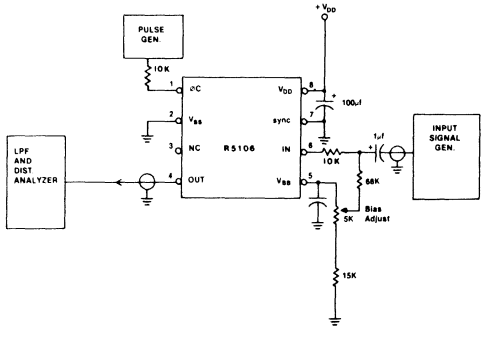

Figure 4. R5106 Test Configuration

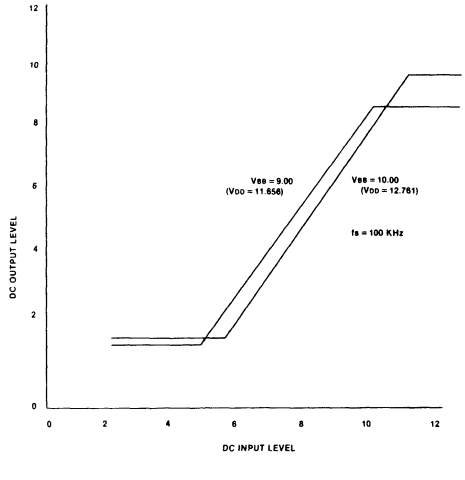

Figure 5. DC Output vs. DC Input, R5106

as a function of f_m/f_s. It also shows typical performance of the R5106 for various sample rates ($f_s = f_c/2$), including the effects of f_m/f_s. Note that, typically, there is less than 1 dB loss in the delay line itself.

Circuit Configuration

The normal operating configuration is shown in Figure 9. The bias should be set such that sine-wave signals large enough to show visible clipping are symmetrically clipped; the clipping should disappear on both top and bottom as the signal level is reduced. A different device, or operation at different sample rates (particularly for changes between widely different sample rates) may require readjustment for optimum performance.

A sync input is included on the device and the waveform is shown in Figure 4. This input allows synchronized operation of multiple devices in either serial or parallel configuration when the same sync pulse is applied to each individual R5106. If the devices are used individually, the sync input (pin 7) should be grounded.

Performance Considerations

The R5106, because of its low cost and clock-fixed delay independent of input frequency, has many applications in the consumer area, particularly for providing delay and its associated effects for audio-frequency devices (e.g., reverberation, vibrato, speed change or corrections, etc.). It is very important to remember that the device is a sampled-data device, and as such has important requirements on filtering of the input and output signals and on control of the clock frequency.

The analog input should be filtered to limit input components to less than $f_{sample}/2$. Normally a stricter limiting is desirable-to a limit more nearly 0.3 f_{sample}. The reason for this requirement is that all input components become modulated by the sampling frequency to generate (f_s-f_m) and also many other products. The result is to "fold" the input about $f_s/2$ so that components above $f_s/2$ reappear on equal distance below $f_s/2$. Limiting the input to $f_s/3$ provides a filter "guard band" to permit adequate attenuation of the otherwise disturbing high-frequency components.

The output should be filtered because, even after the S/H, the output is only stepwise continuous. Clocking steps appear at the times of clock transitions. The high frequencies contained in the abrupt changes are all extraneous and for best performance should be removed by a filter with cut-off at approximately $f_{sample}/2$ or less and rolloff of as much as 36 dB/octave or more. One can move the cutoff frequency by scaling the resistor or capacitor values, or their products (e.g. to double the cutoff frequency to 30 KHz, one halves the resistance or capacitance value). If simple RC filtering is used, note that the output impedance of the R5106 is quite high.

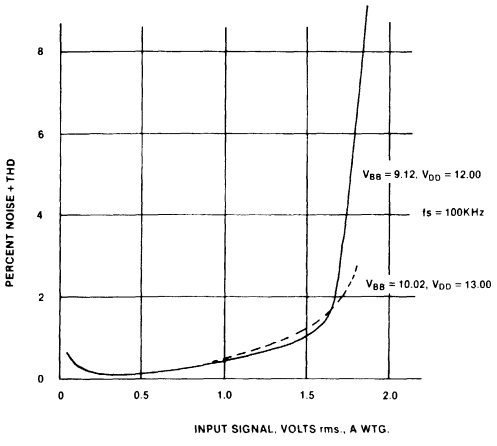

Figure 6. Total Harmonic Distortion + Noise vs. Input Level

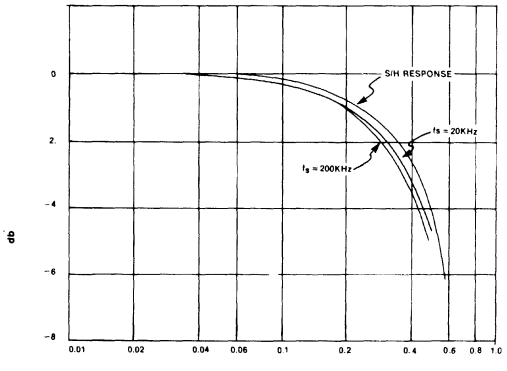

Figure 7. Relative Responses of R5106 vs. Sample Rate, fs

Therefore, the loading impedance should never be less than 100KΩ; otherwise, second order harmonic distortion will become excessive. A simple PNP emitter follower with an Re of 12KΩ will insure a high loading impedance. Also, overload should be avoided because increased signal amplitude near overload gives rise to rapidly increasing high-order intermodulation products which lie within the useful pass band and which thus are not normally reducible by output filtering.

For optimized performance, care should be given to layout and design as well as the filtering requirements. Ground planes are generally required on circuit boards to reduce cross-talk, and shielding of high-impedance circuits, such as the input circuit, is desirable.

For many applications, cost is a more important factor than the ultimate in performance, and relaxed filtering is permissible. However, the user should be well aware of the cost/performance tradeoffs involved.

Evaluation Circuit SC5106

For evaluation purposes or for relatively high-performance operation, a circuit board is available from Reticon. This board encompasses the required filters, operation amplifiers, and ground plane. The schematic is shown in Figure 9. The board provides a variable oscillator for sample frequencies from 20 KHz to 200 KHz. The output filter amplifier is designed as a two-pole, maximally flat filter with a cutoff frequency of 15 KHz. Change in cutoff frequency requires component changes.

The SC5106 board is designed to handle a wide range of bandwidths and clock rates; as a consequence anti-aliasing input filters should be externally provided to limit the input bandwidth to less than $f_{sample}/2$.

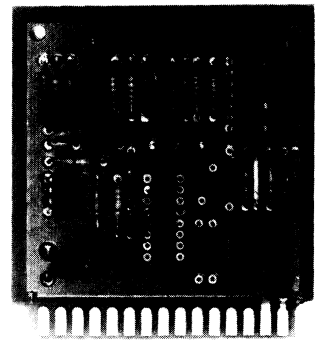

Figure 8. SC5106 Evaluation Circuit

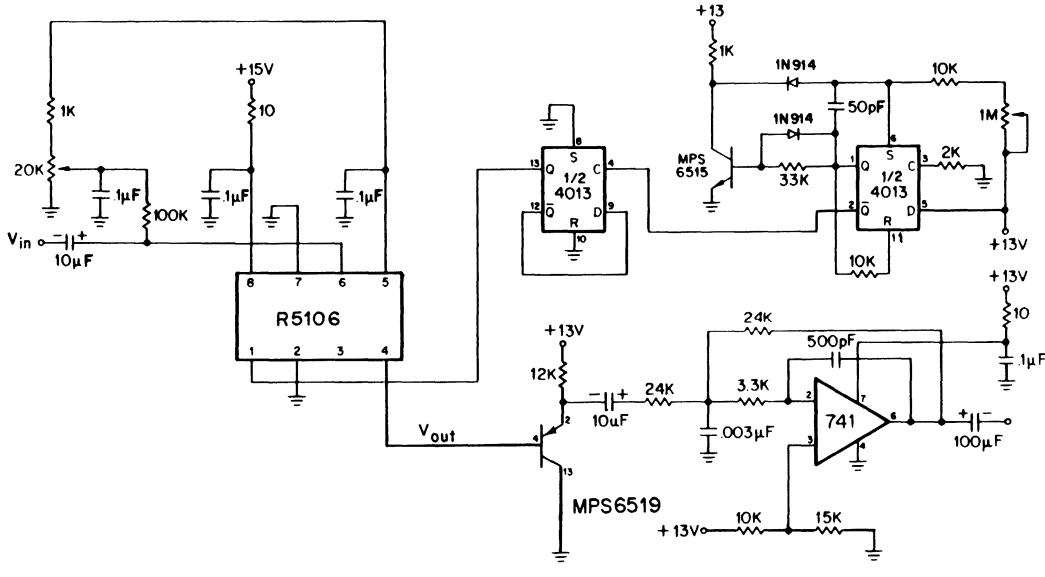

Figure 9. SC5106 Evaluation Circuit Schematic

Table I

Absolute Maximum Rating	Min	Max	Units
Voltage on any terminal with respect to common	-0.4	+18	V
Storage Temperature	-55	+125	°C
Temperature under bias	-55	+85	°C

Caution

Static discharge to any lead of this device may cause permanent damage. Store with shorting clip or inserted in conductive foam. Use grounded soldering irons, tools, and personnel when handling devices. Avoid synthetic fabric smocks and gloves. It is recommended that the device be inserted into socket before applying power. Power supplies should not exhibit turn-on or turn-off spikes. Use decoupling networks to suppress power supply turn on/off transients, ripple and switching transients. Do not apply independently powered or AC coupled signals or clocks to the chip with power off as this will forward bias the substrate. Damage may result if external protection precautions are not taken.

Table II
Device Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Units
Trigger Clock Voltage Amplitude[1]	V_C	2		V_{DD}	Volts
Drain Supply Voltage[1]	V_{DD}	5	12	13	Volts
Tetrode Gate Voltage (see text)	V_{BB}		V_{DD}-2	V_{DD}	Volts
Sampling Frequency (½ External Clock Frequency)	f_S	0.25	50-100	800	KHz
Clock Pulse Width	t_{cp}	200	$t_C/2$	t_C-300	nS
Signal Frequency Bandwidth (3 dB point)		See Fig. 8	$0.4f_S$		
Signal to Noise		See Fig. 5			
Distortion		See Fig. 6			
Gain[2]		0	3		dB
Input Capacitance	C_{in}			15	pF
Input Shunt Resistance[3]	R_{in}	300			Kohms
Optimum Signal Input Bias[4]			7.6		Volts dc
Maximum Input Signal Amplitude[5]		1.0	1.5		Volts rms
Sync Pulse Amplitude		5		V_{DD}	Volts
Clock Input Capacitance	Cc		8	10	pF

Notes: 1. All voltages measured with respect to GND (pin 2).
2. The value of gain depends on the output loading. Values given are for limited external loading.
3. Effective a-c shunt resistance measured at ½ MHz sample rate.
4. The input bias voltage varies with the magnitude of the clock voltage (and V_{DD}) and may be adjusted for optimum linearity at maximum signal level. The value shown is nominal for 12 volt clocks.
5. With V_{DD} = 13V, V_{BB} 10.4, f_S = 100 KHz.