PAiA 4780 Twelve Stage Analog Sequencer Design Analysis

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DESIGN ANALYSIS: CLOCK

As is shown in the block diagram of the sequencer (fig. 1) and the schematic (fig. 2), the clock does a lot more than simply provide timing pulses for the ring counter.

At the heart of the clock is a simple relaxation oscillator built around a single Norton amplifier stage (pins 1, 5 & 6 of IC-l) which is arranged in a Schmitt trigger configuration. Assuming that the RUN/STOP switch is in the "run" position, there are three major bias sources to the inputs of this amplifier. The first is into the non- inverting input (pin 1) through resistor R18. The second is also applied to the non-inverting input and is derived from the normally high output of the amplifier through R16. The third current flows into the inverting input through R34 as a result of the voltage that appears across the timing capacitor C4.

During the major portion of a clock cycle, the combined current flow into the non-inverting input of the amplifier exceeds that which flows into the inverting input and as a result the output of the amplifier is held very close to the positive supply voltage.

As C4 charges through the fixed resistance R35 and the front panel rate control R135 the voltage across it eventually becomes such that the resulting current flow through R34 exceeds the combined current flow of R18 and R16 and at this point the output of the amplifier switches to a low state. Two things happen simultaneously. The current that was flowing through R16 is removed so that the current through R34 will have to increases significantly before the amplifier can switch again ad diode D1 becomes forward biased and begins to discharge C4.

As C4 discharges, its voltage soon reaches the point at which the current through R34 is less than that through Rl8 causing the amplifier's output to once again switch high. This simultaneously reverse biases D1 and re-establishes the feed- back current through R16. From this point the cycle repeats.

The minimum width of the negative going clock pulses that appear at pin 5 of IC-l is limited by the dynamic impedance of diode Dl and while they are relatively short (about 1% of the total period at the slowest clock rate) they are far too long to use directly on the clock line. The clock pulses are differentiated by C1 and R15 and used to switch a second amplifier section of IC-l (pins 10. 11, and 12). The output of this amplifier stage is once again high riding with micro- second range pulses to ground.

Switching the RUN/STOP switch to the "stop" position introduces a fourth bias current to the amplifier in the relaxation oscillator by raising the ungrounded side of R30 to the positive supply voltage The resulting current flow through R31 and R13 is such that the total current flow into the non-inverting input of the amplifier is much greater than the current produced by the highest voltage that C4 can charge to. The output of the amplifier cannot switch to its low state and the clock can be considered off.

The fourth bias current can be removed, and the clock started, either by returning S1 to the "run" position or by turning on transistor Q2, thereby shorting the junction of R19 and R31 to ground. Q2 can

be turned on and held on by applying a positive voltage to the "run" input jack on the front panel or it can be turned on for very short periods of time for synchronization purposes by applying pulses to the "synch" input pin Jack- Pulses applied to the "synch" input are differentiated by capacitor C3 with the negative going spikes at the trailing edges of the pulses clamped to ground by D2.

To examine the operation of this comparator, assume that the relaxation oscillator is at the point where it is just ready to fire and produce a clock pulse. At this point, the output of the comparator is low because there is greater current now into pin 3 than pin 2. As soon as the output of the relaxation oscillator (pin 5) goes low, the current that was flowing through R39 is removed without the current contribution of R39, there is greater current flow into the non-inverting input than the inverting input and the output of the comparator switches to its high state causing a voltage step to appear at the step trigger output.

The output of the relaxation oscillator quickly returns to its normal high state but at the time that it does, the voltage appearing across C4 is considerably lower than it was at the point of firing. Even through the current flow through R39 is restored, there is still greater current flow into pin 2 of the comparator than pin 3 because of the reduced current flow through R38. As the voltage across C4 increases, the point is eventually reached at which the currents through R38 and R39 exceed that through R136 and the output of the comparator returns to its low state removing the voltage step at the output. The point at which this transition to a low state occurs is a function of how high the voltage across C4 has to rise before the inverting current exceeds the non- inverting input current and this in turn is dependent on the setting of the front panel DURATION control.

When the output of the comparator switches high, the leading edge of the step is differentiated to a pulse by C7 and appears at the front panel pulse trigger output jack. The negative spike that would appear at the trailing edge of the step is clamped to ground by D3.

The step trigger also directly drives the light emitting diode LED-13 which indicates to the user the duration of the step trigger output. In order to ease power supply regulation requirements, the relatively heavy periodic current flow required to light the LED is balanced by switching the dummy load R24 "on" anytime that the LED is off. The inversion required to perform this is provided by the fourth stage of the amplifier in the IC-l package, pins 8, 9 and 13.

RING COUNTER

The design of the ring counter section of the sequencer is a common concept employing 12 serially coupled latches. A partial schematic and typical stage are shown in figs 3 & 3a. Like any other latch, this circuit has two stable states. When the output voltage of the amplifier is low there is no current flow through the feedback resistor Rf and the greater current into the inverting input through Rb than through Rc into the non-inverting input causes the output to stay low.

Once the circuit changes state to a high output a current begins to flow through Rf which when added to the current already flowing through Rc results in a greater total flow into the non-inverting input than is provided to the inverting input through Rb. The result is that the output stays high.

This stage can be "set" or "loaded" (output changed to a high state) by momentarily decreasing the current flow into the inverting input. This is the case when the series capacitance and resistance (R1/C1) are connected to the output of another latch whose output is transitioning from a high to a

low state. Once set, the stage can be reset by momentarily dropping the clock line from positive supply to ground,

If the time constant of R1/C1 is chosen such that it is long when compared to the duration of the clock pulse, a ring of these stages will count by advancing the high state from one stage to the next each time there is a clock pulse. In the process of being reset, each stage passes the count to the stage immediately following it in the chain.

The entire chain can be cleared by holding the clock line at ground for a period of time greater than the time constant of the R1/C1 combination. When the RUN/STOP switch is set to the "stop/clear" position, the series combination of R29 and C5 on the clock board generates a relatively long (0.5 sec. approximately) current pulse that turns on transistor Ql which in turn shorts the clock line to ground.

It is undesirable to have more than a single stage of the counter set at any given time, yet this situation would naturally occur if the output of an intermediate stage of the counter was fed back into the input. To prevent this, the output of stage one serves as a reset for the rest of the stages.

When stage one goes high, current supplied to the inverting inputs of the rest of the stages in the counter by way of R111 - R121 causes each stage to reset.

The first stage of the counter can be set in a variety of ways. Pressing the front panel LOAD push-button causes a voltage to appear across R133 on the clock board which is coupled to the non-inverting input of the first counter stage by means of C2 3 and Rl34. Applying a voltage step to the front panel RUN input jack produces an identical result because of diode D5 (but note that pressing the LOAD button reverse biases D5 and will not cause the clock to run). Setting the RUN/STOP switch to the "run" position causes a voltage to appear across R62 which when coupled through C8 and R184 produces the same results.

Taking the first as typical, the output of each of the counter stages is connected through a current limiting resistor (R7) to a light emitting diode (LED-1). All of the LEDs in turn connect to a common line that returns to ground through the zener diode D4. These LEDs and the zener perform a number of junctions.

First, the LEDs light to indicate to the user which stage is currently loaded. Second, the LED and zener together serve to clamp the voltage that appears across the voltage divider at the output of each stage (R41 in stage 1) to a reference level of approximately 6 volts and thereby assists in eliminating voltage drift at the control voltage output of the sequencer. Third, the LEDs function as normal diodes to prevent interaction between the twelve counter stages. Finally, the voltage that appears across the zener any time that any of the ring counter stages are set serves as a signal back to the clock that the counter is loaded.

The multi-turn potentiometers at the output of each stage of the counter are resistance coupled (Rl in stage 1) to a common line that feeds non-inverting summing amplifier IC-5. The output of the summing amplifier is connected to the glide circuit consisting of the front panel GLIDE control R137 and capacitor C2. The emitter follower Q4 serves as an output buffer to minimize unwanted control voltage level changes that could otherwise be a side effect of changing the glide rate.

In the "conditional run" (middle) setting of the clock's RUN/STOP switch, the clock runs only when there is a "1" loaded into the ring counter. This is accomplished by using the voltage that appears across the zener diode D4 when any stage of the counter is high (see ring counter analysis) to turn on transistor Q3 on the look board. As long as Q3 is on, the voltage divider R21 and R20 in the clock is connected between positive supply and ground causing a normal bias current to flow through RI8. When Q3 turns off, the voltage divider is no longer grounded causing the junction of R21 and R20 to rise to essentially supply thereby forcing 4 times more current to flow through RI8 than previously. As explained previously, this stops the action of the relaxation oscillator. When the RUN/STOP switch is in the "run" position the current to hold Q3 on is supplied through R141.

A third amplifier in IC-1 (pins 2, 3 and 4) takes care of generating the step and pulse trigger outputs of the sequencer, This amplifier is wired as a comparator so that its output voltage (at pin 4) is low until the sum of the currents into the noninverting input through R38 and R39 falls below the level of the reference current through R136.

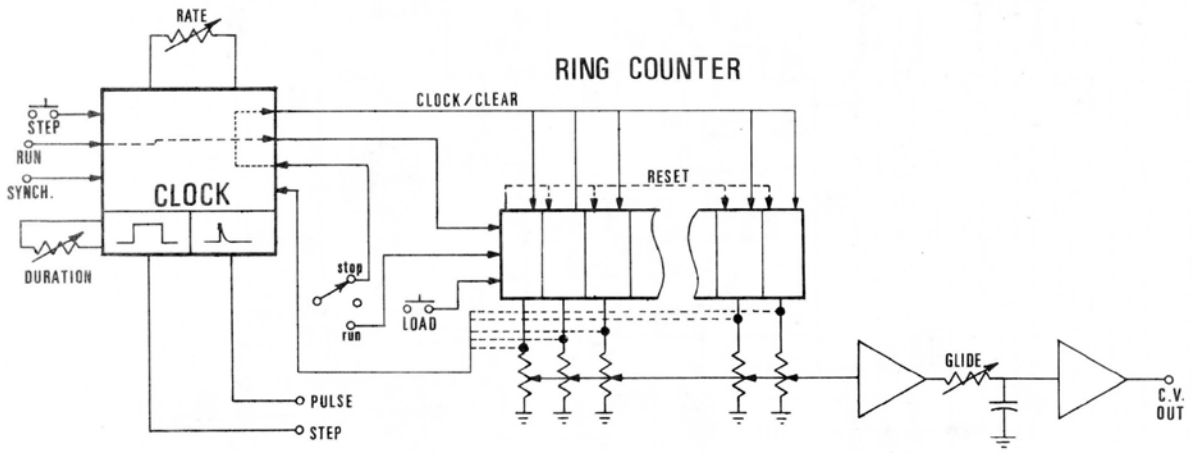

Figure 1. PAiA 4780 Sequencer Block Diagram

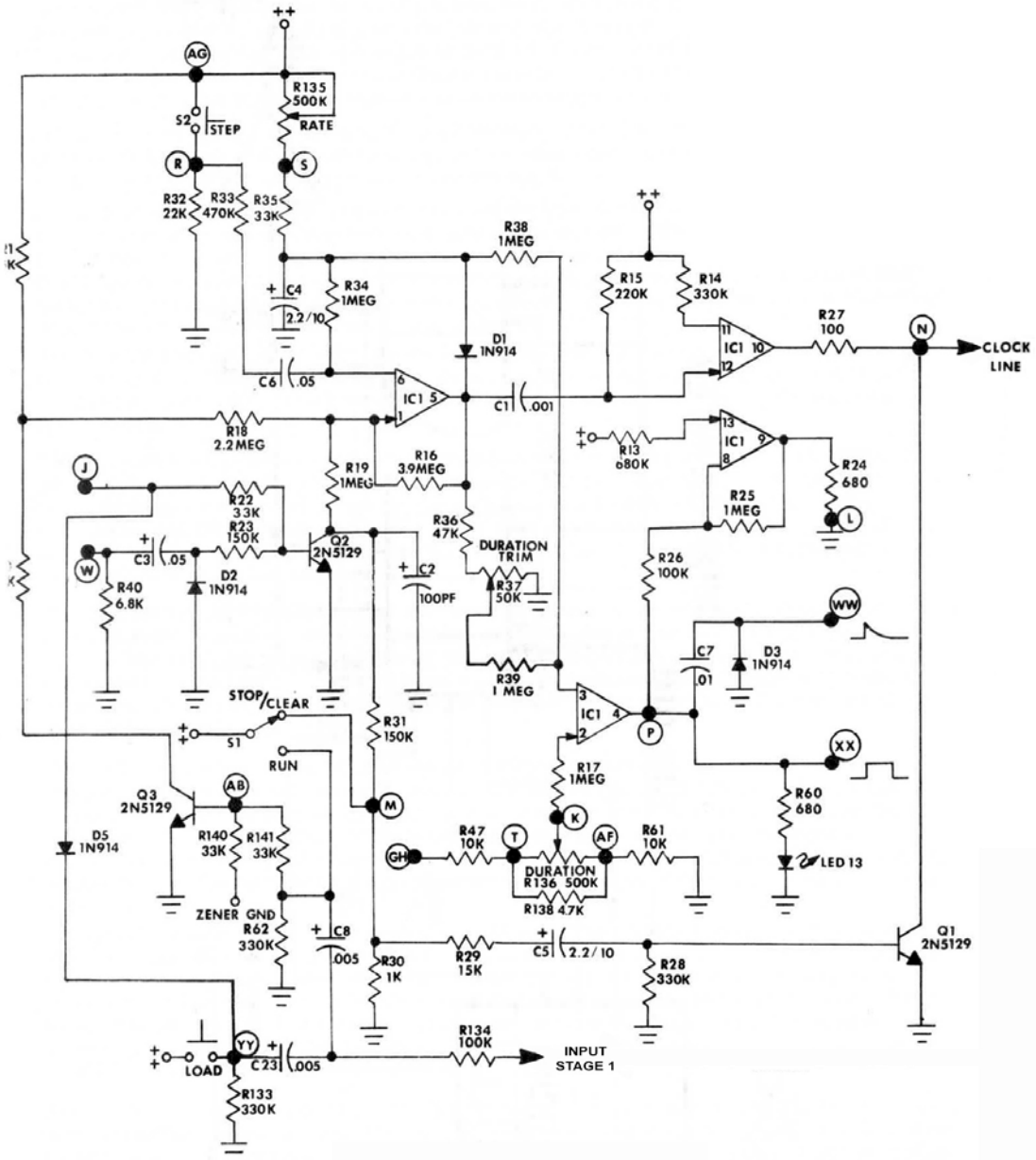

Figure 2. Sequencer Clock Circuitry

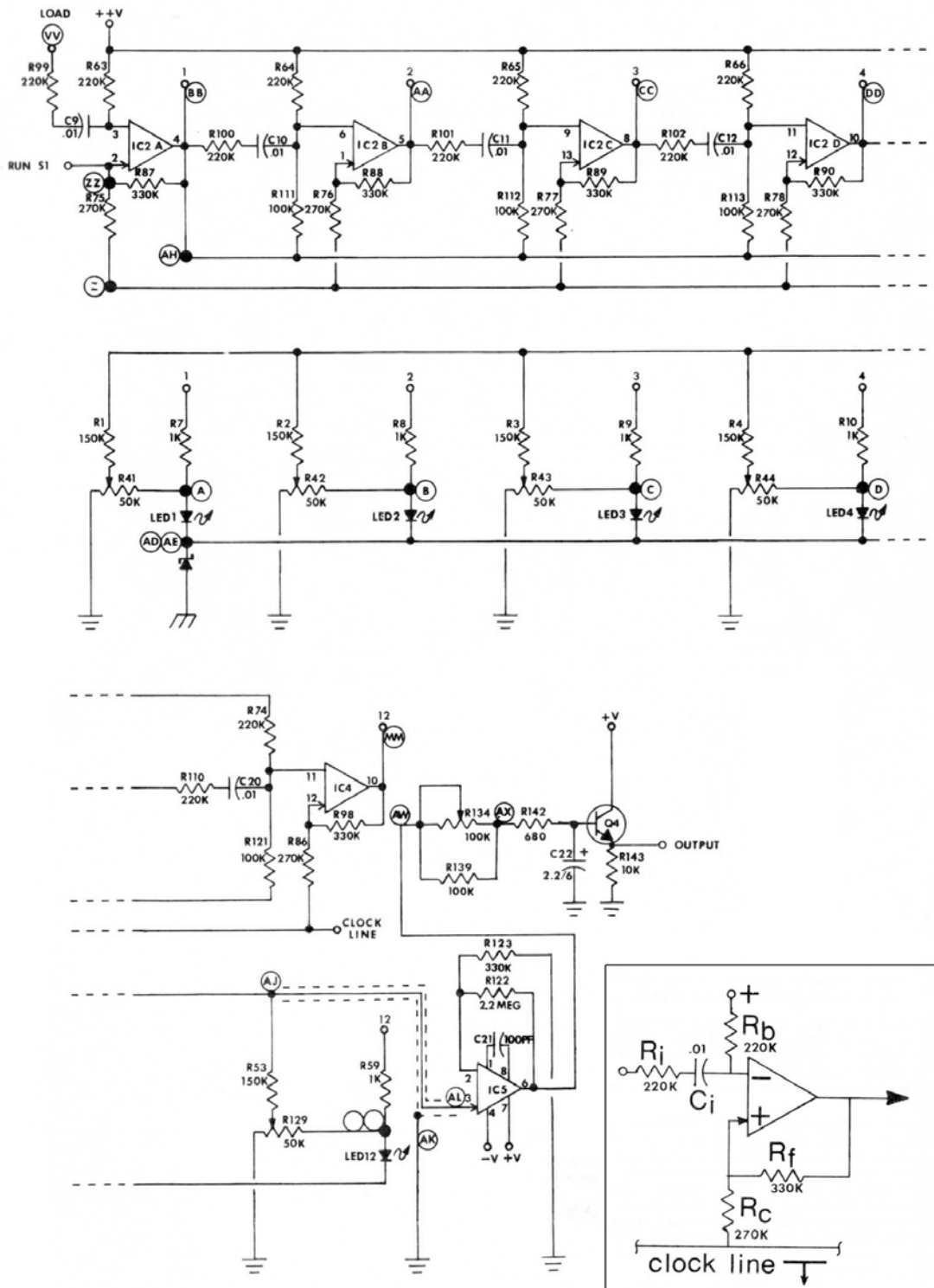

Figure 3. Ring Counter, CV Out Schematic

Fig 3a. Typical counter stage